WHAT IS CLAIMED IS:

1. A method of forming a MOSFET device in an integrated circuit, the method comprising:

forming a relatively thin dielectric layer on a surface of a substrate;

forming a first region of relatively thick material having a predetermined lateral length on the surface of the substrate adjacent the relatively thin dielectric layer;

implanting dopants of a first conductivity type in the substrate to form a first top gate using a first edge of the first region as a mask to define a first edge of the first top gate; and

implanting dopants of a second conductivity type with high dopant density to form a drain contact using a second edge of the first region as a mask to define a first edge of the drain contact, wherein the distance between the first top gate and drain contact is defined by the lateral length of the first region.

2. The method of claim 1, further comprising:

depositing a gate material layer on the relatively thin dielectric layer, wherein an edge of the gate material layer is used to form a second edge of the first top gate so that the first top gate is formed between the gate material layer and the first region of relatively thick masking material.

3. The method of claim 1, wherein the drain contact is formed deeper from the surface of the substrate than the first top gate and has a higher doping density at every depth than the first top gate.

4. The method of claim 1, further comprising:

implanting dopants of a second conductivity type in the substrate using the first region as a mask to form first and second drift regions.

5. The method of claim 4, further comprising,

forming a well of the second conductivity type in the substrate under the first region to reduce resistance in the first and second drift regions.

6. The method of claim 4, further comprising:

diffusing the dopants that make up the first and second drift regions to overlap under the first region to form a continuous drain extension region that extends laterally from under the first top gate past the drain contact.

7. The method of claim 6, further comprising,

forming a well of the second conductivity type in the substrate under the first region to reduce resistance in the first and second drain extensions.

8. The method of claim 1, further comprising:

forming a second region of relatively thick material on the surface of the substrate adjacent the relatively thin dielectric layer, the second region is connected to the first region, the first and second regions forming a central opening, wherein the drain contact is formed through the central opening.

9. The method of claim 8, wherein the first and second regions are first and second relatively thick dielectric layers.

10. The method of claim 8, further comprising:

implanting dopants of the first conductivity type to form a second top gate using a second edge of a potion of the second region as a mask to defined a first edge of the second top gate, wherein the distance between the second top gate and the drain contact is defined by the lateral distance of the portion of second region.

11. The method of claim 8, wherein the first top gate extends around an outer perimeter of the first and second regions.

12. The method of claim 8, further comprising:

implanting dopants of the second conductivity type in the substrate using the first and second regions as a mask to form first, second and third drift regions.

13. The method of claim 12, further comprising:

diffusing the dopants that make up the first, second and third drift regions to overlap under the respective first and second regions to form a continuous main drift region.

14. The method of claim 12, further comprising,

forming a well of the second conductivity type in the substrate to reduce resistance in the in the first, second and third drift regions that extends from a portion of the first top gate to a portion of the second top gate.

15. The method of claim 8, wherein the first and second regions are first and second gate material layers.

16. The method of claim 15, wherein the first and second gate material layers are left floating.

17. The method of claim 15, further comprising:

coupling the first and second gate material layers to the drain contact.

18. A method of forming a lateral MOSFET device in an integrated circuit, the method comprising:

forming a dielectric layer on a surface of a substrate, wherein the dielectric layer has a relatively thick dielectric region and a relatively thin dielectric region;

forming a gate electrode overlaying a portion of the relatively thin dielectric region;

introducing a first conductivity type dopant to form a top gate region along the surface of the substrate, wherein a first edge of the top gate region is defined by a

second edge of the gate electrode and a second edge of the top gate region is defined by a first edge of the relatively thick dielectric region;

introducing a second conductivity type dopant with a high dopant density to form a first region of the second conductivity type along the surface of the substrate, wherein an edge of the first region is defined by a second edge of the relatively thick dielectric region; and

wherein the first region is separated from the top gate region by the approximate lateral distance between the first edge of the relatively thick dielectric region and the second edge of the relatively thick dielectric region.

19. The method of claim 18, wherein the relatively thick dielectric region is formed with a central opening that defines the first region, further wherein the first edge of the relatively thick dielectric region is an outer perimeter of the relatively thick dielectric region and the second edge of the relatively thick dielectric region is an inner perimeter of the relatively thick dielectric region.

20. The method of claim 18, wherein the gate electrode is a poly silicon gate that is deposited on the surface portion of the relatively thin dielectric region.

21. The method of claim 18, wherein forming the dielectric layer further comprises:

depositing a relatively thick dielectric layer on the surface of the substrate;

etching the relatively thick dielectric layer to create the relatively thick dielectric region; and

growing the relatively thin dielectric region on the surface of the substrate.

22. The method of claim 18, wherein the relatively thin dielectric layer is formed by oxidation of the substrate.

23. The method of claim 18, wherein the relatively thick dielectric region is formed by local oxidation.

24. The method of claim 23, wherein the relatively thin dielectric region is formed after the formation of the relatively thick dielectric region.

25. The method of claim 18, further comprising:

introducing second conductivity type dopant into the substrate to form a drift region of the second conductivity type before the first region is formed, wherein the first region is formed in the drift region.

26. The method of claim 25, wherein forming the drift region further comprises:

depositing a relatively thick dielectric region on the surface of the substrate;

removing a portion of the relatively thick region from the surface of the substrate; and

using the remaining portion of the relatively thick oxide layer as a mask when introducing the second conductivity type to form the drift region.

27. The method of claim 25, wherein the drift region is formed before the dielectric layer is formed.

28. The method of claim 27, wherein a portion of the relatively thick region of the dielectric layer is formed over the drift region.

29. The method of claim 18, further comprising:

introducing a first conductivity type dopant in the substrate to form a body; and

introducing a second conductivity type dopant with high dopant density in the body to form a second region, wherein a second edge of the second region is formed by using a first edge of the gate electrode as a self-aligned mask edge.

30. The method of claim 29, wherein the second region is a source and the first region is a drain.

31. The method of claim 29, further comprising:

introducing a first conductivity type dopant with high dopant density in the body to form a body contact.

32. The method of claim 31, further comprising:

removing portions of the relatively thin dielectric regions that are adjacent the body contact, the first region, the second region and the gate electrode.

33. The method of claim 18, further comprising:

introducing dopant of the second conductivity type into the substrate to form first and second drift regions using the relatively thick dielectric region as part of a mask.

34. The method of claim 33, further comprising:

diffusing the first and second drift regions to form an overlap third region under the relatively thick dielectric region, wherein the first, second and third drift regions extend laterally from the gate electrode beyond the first region.

35. The method of claim 34, further comprising:

forming a well region in the substrate of the same conductivity type as the first and second drift regions to reduce resistance within the first and second drift regions, wherein portions of the first and second drift regions are formed in the well.

36. The method of claim 33, wherein the first and second drift regions are spaced apart from each other by the width of the relatively thick dielectric region.

37. A method of making a high voltage lateral MOSFET for an integrated circuit, the method comprising:

forming a relatively thick dielectric layer on a surface of a substrate;

removing portions of the relatively thick dielectric layer to form a relatively thick dielectric region of a predetermined lateral length;

implanting second conductivity type dopants with high dopant density in the substrate to form a drain region using a second edge of the relatively thick dielectric layer as a mask to form a first edge of the drain region;

implanting first conductivity type dopants in the substrate to form a top gate using a first edge of the relatively thick dielectric layer as a mask to form a second edge of the top gate, wherein the distance between the first edge of the drain region and the second edge of the top gate is defined by the length of the relatively thick dielectric layer; and

implanting second conductivity type dopants with high dopant density in the substrate to form a source region, wherein the top gate is positioned between the source region and the drain region.

38. The method of claim 37, further comprising:

implanting the first conductivity type dopants to form a body region adjacent the surface of the substrate and the source region; and

implanting the first conductivity type dopants with high dopant density in the body region and adjacent a portion of the source region to form a body contact.

39. The method of claim 37, wherein the drain region is formed to extend deeper from the surface of the substrate than the top gate, further wherein the drain region is formed with a higher doping density at every depth from the surface of the substrate than the top gate.

40. The method of claim 37, further comprising

forming a relatively thin dielectric layer on the surface of the substrate; and

depositing a gate electrode overlaying a portion of the thin dielectric layer

41. The method of claim 40, further comprising:

using a mask to form a first edge of the source area; and

using a first edge of the gate electrode as a self-aligning mask to form a second edge of the source area.

42. The method of claim 40, further comprising:

using a second edge of the gate electrode as a self-aligning mask to form a second edge of the top gate.

43. The method of claim 37, further comprising:

forming a first drift region of a second conductivity type in the substrate using a first edge of the relatively thick dielectric region as a mask; and

forming a second drift region of a second conductivity type in the substrate using a second edge of the relatively thick dielectric region as a mask.

44. the method of claim 43, further comprising:

diffusing the first and second drift regions laterally under the relatively thick dielectric layer to create an overlap region under the relatively thick dielectric layer.

45. The method of claim 43, further comprising:

forming a well of the second conductivity type in the substrate to reduce resistance within the first and second drift regions, wherein portions of the first and second drift regions are formed in the well.

46. A method of forming a high voltage MOSFET for an integrated circuit, the method comprising:

forming a relatively thin layer of dielectric on a surface of a substrate;

depositing a gate material layer on the relatively thin layer of dielectric;

removing portions of the gate material layer to form a first and second gate material regions of predetermined lateral lengths;

introducing a first conductivity type dopant in the substrate to form a top gate using first edges of the first and second gate material regions as masks, wherein the

top gate is formed adjacent the surface of the substrate and laterally between the first and second gate material regions;

introducing a second conductivity dopant of high dopant density in the substrate to form a drain region adjacent the surface of the substrate using a second edge of the second gate material region as a mask to form a first edge of the drain region, wherein the second gate material region is positioned laterally between the drain region and the top gate; and

wherein the spaced distance between the top gate and the drain region is determined by the lateral length of the second gate material region.

47. The method of claim 46, wherein the drain region is formed to extend deeper from the surface of the substrate than the top gate, further wherein the drain region is formed with a higher doping density at every depth than the top gate.

48. The method of claim 46, wherein the removing of portions of the gate material layer further forms a third gate material region of a predetermined lateral length, wherein a edge of the third gate material region is used as a mask to form a second edge of the drain region.

49. The method of claim 48, wherein the second and third gate material regions are left floating.

50. The method of claim 48, further comprising:

coupling the second and third gate material regions to the drain contact.

51. The method of claim 48, wherein the third gate material region is connected to the second gate material region, the second and third gate material regions forming a central opening, wherein the drain region is formed through the central opening.

52. The method of claim 46, further comprising:

introducing the second conductivity type dopant of high density to the substrate to form a source region adjacent the first gate material region, wherein the first gate material region is generally positioned laterally between the source region and the top gate.

53. The method of claim 52, wherein an edge of the first gate material region is used as a mask to form an edge of the source region.

54. The method of claim 52, further comprising:

introducing the first conductivity type dopant to the substrate to form a body region, the body region being positioned adjacent the surface of the substrate and the source; and

introducing a first conductivity dopant of a high density in the body region to form a body contact, wherein the body contact is positioned adjacent the surface of the substrate and a portion of the source.

55. The method of claim 46, further comprising:

forming a first drift region of a second conductivity type dopant in the substrate using a first edge of the second gate material region as a mask; and

forming a second drift region of the second conductivity type dopant in the substrate using a second edge of the second gate material region as a mask.

56. The method of claim 55, further comprising:

diffusing the first and second drift regions to form an overlap third region under the second gate material region.

57. The method of claim 55, further comprising:

forming a well region in the substrate of the second conductivity type to reduce resistance within the first and second drift regions, wherein portions of the first and second drift regions are formed in the well.

58. The method of claim 55, wherein the first and second drift regions are spaced apart from each other by the width of the second gate material region.

59. A method of forming a lateral MOSFET in an integrated circuit, the method comprising:

forming a drain contact of a second conductivity type with a high density dopant in a substrate adjacent a surface of the substrate;

forming a top gate of a first conductivity type in the substrate adjacent the surface of the substrate and a predetermined distance from the drain contact after the drain contact is formed; and

wherein the drain contact is formed to extend deeper from the surface of the substrate than the top gate and is formed to have a higher dopant density at every depth than the top gate so a mask is not needed to shield the drain contact from the first conductivity dopants during formation of the top gate.

60. The method of claim 59, further comprising:

forming a relatively thin dielectric layer on a surface of a substrate, the substrate being of a first conductivity type with a low dopant density; and

depositing a gate on the surface on the relatively thin dielectric layer.

61. The method of claim 59, further comprising:

forming a source of the second conductivity type with a high dopant density in the substrate approximate the gate, wherein the source is formed to extend deeper from the surface of the substrate than the top gate and is formed to have a higher dopant density at every depth than the top gate so a mask is not needed to shield the source from the first conductivity dopants during formation of the top gate.

62. The method of claim 59, wherein forming the distance between the drain contact and the top gate further comprising:

forming a relatively thick layer of material having a predetermined lateral length on the surface of the substrate;

introducing high density dopants of the second conductivity type to the substrate to form the drain contact, wherein a first edge of the relatively thick layer of material defines a first edge of drain contact; and

introducing dopants of the first conductivity type to the substrate to form the top gate, wherein a second edge of the relatively thick layer of material defines a first edge of the top gate, further wherein the distance between the top gate and the drain contact is defined by the lateral length of the relatively thick layer of material.

63. The method of claim 62, wherein the relatively thick layer of material is a layer of dielectric.

64. The method of claim 62, wherein the relatively thick layer of material is a layer of gate material.

65. A method of forming a pn junction diode in an integrated circuit, the method comprising:

forming a first region of relatively thick material on the surface of a substrate;

forming a second region of relatively thick material on the surface of a substrate a predetermined distance from the first region;

implanting high density of dopants of a second conductivity type in the substrate to form a cathode contact using first edges of the first and second regions as masks to define edges of the cathode contact, wherein the cathode contact is positioned between the first and second regions; and

implanting dopants of a first conductivity type in the substrate to form first and second top gate regions using second edges of the first and second regions as masks to define first edges of the first and second top gate regions, wherein the distance between the cathode contact and the first top gate region is defined by the lateral length of the first region and the distance between the cathode contact and the second top gate region is defined by the lateral length of the second region.

66. The method of claim 65, further comprising:

implanting high density dopants of the first conductivity type in the substrate to form at least one anode contact regions.

67. The method of claim 65, further comprising:

implanting dopant of the second conductivity type in the substrate to form drift regions; and

diffusing the dopant of the second conductivity type that forms the drift regions so that the drift regions overlap under a respective one of the first and second regions to form a single main drift region.

68. The method of claim 65, wherein the first and second regions are formed with gate material.

69. The method of claim 65, wherein the first region is coupled to the second region, further wherein the first and second regions form a central opening defining the cathode contact.

70. The method of claim 69, wherein the first and second top gate regions extend around an outer perimeter of the first and second regions.

71. The method of claim 65, wherein the first and second regions are formed with dielectric material.

72. The method of claim 71, wherein the first and second regions are formed by local oxidation.

73. A method of forming a high voltage bipolar transistor in an integrated circuit, the method comprising:

forming a first region of relatively thick material on a surface of a substrate;

forming a second region of relatively thick material on the surface of the substrate a predefined distance from the first region;

introducing dopant of a second conductivity type to form a base region in the substrate using first edges of the first and second regions to form edges of the base region, wherein the base region is positioned between the first and second regions;

introducing dopants of a first conductivity type to form a first top gate using a second edge of the first region as a mask to form an edge of the first top gate, wherein the distance between the first top gate and the base region is defined by the lateral length of the first region; and

introducing dopants of the first conductivity type to form a second top gate using a second edge of the second region as a mask to form an edge of the second top gate, wherein the distance between the second top gate and the base region is defined by the lateral length of the second region.

74. The method of claim 73, further comprising:

introducing high density dopant of the second conductivity type in the base region to form a base contact;

introducing high density dopant of the first conductivity type in the base region to form an emitter; and

introducing high density dopant of the first conductivity type into the substrate adjacent the second top gate to form a collector contact.

75. The method of claim 73, further comprising:

introducing dopant of the second conductivity type into the substrate; and

diffusing the dopant of the second conductivity type, wherein the dopant of the second conductivity type diffuses under the first and second regions to form a single drift region that extends from a portion of the first top gate to a portion of the second top gate.

76. The method of claim 73, wherein the first and second regions are made of a gate material.

77. The method of claim 73, wherein the first and second regions are made of a dielectric material.

78. The method of claim 77, wherein the first and second regions are formed by local oxidation.

79. A lateral MOSFET for an integrated circuit comprising:

a substrate;

a relatively thin layer of dielectric formed on a surface of the substrate;

a first region of relatively thick material formed on the surface of the substrate adjacent the relatively thin dielectric material having a predefined lateral length, wherein the first region can mask dopants from penetrating the surface of the substrate;

a drain contact region of a second conductivity type with high dopant density formed in the substrate adjacent the surface of the substrate; and

a first top gate of a first conductivity typed formed in the substrate adjacent the surface of the substrate, the distance between the drain contact region and the first top gate is defined by the lateral length of the first region.

80. The lateral MOSFET for an integrated circuit of claim 79, further comprising:

a gate material region formed on the relatively thin dielectric material, wherein the gate material is used as a mask to form a second edge of the first top gate.

81. The lateral MOSFET of claim 79, further comprising:

a body region of the first conductivity type formed in the substrate adjacent the surface of the substrate;

a source of the second conductivity type with high dopant density formed in the body region; and

a body contact of the first conductivity type with high dopant density formed in the body region adjacent the source.

82. The lateral MOSFET of claim 79, wherein the drain contact region is formed deeper from the surface of the substrate than the first top gate, further wherein the drain contact has a higher dopant concentration at every depth from the surface of the substrate than the first top gate.

83. The lateral MOSFET of claim 79, further comprising:

a main drift region of the second conductivity type formed around the first top gate and extending beyond the drain contact.

84. The lateral MOSFET of claim 83, wherein the main drift region further comprises:

a first drift region formed by implanting dopants of the second conductivity type into the substrate using a first edge of the first region as a mask; and

a second drift region formed by implanting dopants of the second conductivity type into the substrate using a second edge of the first region as a mask, wherein the dopants of the first and second drift regions are diffused under the first region to form the main drift region.

85. The lateral MOSFET of claim 83, further comprising:

a well of the second conductivity type formed under first region to reduce resistance in the main drift region.

86. The lateral MOSFET of claim 79, further comprising:

a first drift region of the second conductivity type in the substrate extending from the first edge of the first region to beyond the first top gate; and

a second drift region of the second conductivity type extending from the second edge of the first region beyond the drain contact.

87. The lateral MOSFET of claim 86, further comprising:

a first conductivity well of the second conductivity type formed under first region in the substrate to reduce resistance in the first and second drift regions.

88. The lateral MOSFET of claim 79, further comprising:

a second region of relatively thick material formed on the surface of the substrate a predetermined distance from the first region, wherein the lateral length of the drain contact region is defined by the distance between the first and second regions.

89. The lateral MOSFET of claim 88, further comprising:

a second top gate of the first conductivity type formed in the substrate adjacent the surface of the substrate, wherein the distance between the drain contact region and the second top gate is defined by the lateral length of the second region.

90. The lateral MOSFET of claim 88, wherein the first region of relatively thick material is connected to the second region of relatively thick material, the first and second regions of relatively thick material having a central opening, the drain contact region is positioned adjacent the central opening.

91. The lateral MOSFET of claim 90, wherein the first top gate extends around an outer perimeter of the first and second regions of relatively thick material.

92. The lateral MOSFET of claim 89, wherein the drain contact region is formed deeper from the surface of the substrate than the first and second top gates and has a higher dopant concentration at every depth than first and second top gates.

93. The lateral MOSFET of claim 89, wherein the first and second relatively thick materials are made from a dielectric material.

94. The lateral MOSFET of claim 89, wherein the first and second relatively thick materials are made from a gate material.

95. The lateral MOSFET of claim 94, wherein the first and second regions are left floating.

96. The lateral MOSFET of claim 94, wherein the first and second regions are coupled to the drain contact region.

97. A lateral MOSFET for an integrated circuit comprising:

a substrate;

a relatively thick dielectric region formed on a surface of the substrate, the relatively thick dielectric region having a predetermined lateral length;

a relatively thin dielectric region formed on the surface of the substrate;

a gate electrode deposited on the relatively thin dielectric region;

a first top gate region of a first conductivity type formed in the substrate adjacent the surface of the substrate and between the gate electrode and the relatively thick dielectric region;

a drain region of a second conductivity type having a high doping density formed in the substrate adjacent the surface of the substrate and adjacent the relatively thick dielectric region, wherein the lateral width of the relatively thick dielectric region defines the lateral distance between the first top gate region and the drain region; and

a source region of the second conductivity type having a high doping density formed in the substrate adjacent the surface of the substrate, wherein the gate electrode is laterally positioned between the source region and the first top gate.

98. The lateral MOSFET for an integrated circuit of claim 97, further comprising:

a body region of the first conductivity type formed in the substrate adjacent the surface of the substrate and the source region; and

a body contact of the first conductivity type having a high dopant density formed in the body region adjacent the surface of the substrate and a portion of the source region.

99. The high power lateral MOSFET for an integrated circuit of claim 97 further comprising:

a drift region of the second conductivity type formed in the substrate adjacent a surface of the substrate and the first top gate and drain region.

100. The lateral MOSFET for an integrated circuit of claim 97, wherein the drain region is formed to extend deeper from the surface of the substrate than the first top gate, further wherein the drain region is formed with a higher doping density at every depth than the first top gate.

101. The lateral MOSFET for an integrated circuit of claim 97, wherein the source region is formed to extend deeper form the surface of the substrate than the first top gate, further wherein the source region is formed with a higher dopant density at every depth than the first top gate.

102. The lateral MOSFET for an integrated circuit of claim 97, further comprising:

a first drift region of the second conductivity type formed in the substrate adjacent the relatively thick dielectric layer and the drain region; and

a second drift region of the second conductivity type formed in the substrate adjacent the first top gate and the relatively thick dielectric layer, wherein the first and second drift regions overlap under the relatively thick dielectric layer.

103. The lateral MOSFET for an integrated circuit of claim 102, further comprising:

a well of the second conductivity type formed in the substrate adjacent the overlapping area of the first and second drift regions to reduce resistance in the first and second drift regions.

104. The lateral MOSFET for an integrated circuit of claim 102, further comprising:

a second top gate of the first conductivity type formed in the substrate adjacent the surface of the substrate and a predetermined distance from the drain region to form a single multistripe device in the integrated circuit, wherein the well extends from a portion of the first top gate to a portion of the second top gate.

105. The lateral MOSFET for an integrated circuit of claim 97, wherein the relatively thick dielectric region has a central opening, the drain region is laterally positioned in the central opening.

106. The lateral MOSFET for an integrated circuit of claim 105, wherein the first top gate is laterally positioned around an outside perimeter of the relatively thick dielectric region.

107. A solid state relay integrated circuit comprising:

a photo diode stack to drive a voltage having a first output and a second output;

a first high voltage MOSFET having a gate, source and drain, the gate of the first high voltage MOSFET is coupled to the first output of the photo diode stack, the source of the first high voltage MOSFET is coupled to the second output;

a second high voltage MOSFET having a gate, source and drain, the gate of the second high voltage MOSFET is coupled to the first output of the photo diode stack, the source of the second high voltage MOSFET is coupled to the second output of the photo diode stack; and

wherein the first and second high voltage MOSFETs comprise,

a substrate,

a relatively thin layer of dielectric formed on a surface of the substrate,

a first region of relatively thick material formed on the surface of the substrate adjacent the relatively thin dielectric material having a predefined lateral length, wherein the first region can mask dopants from penetrating the surface of the substrate,

a drain contact region of a second conductivity type with high dopant density formed in the substrate adjacent the surface of the substrate, wherein the first region is used as a mask to form a first edge of the drain contact, and

a first top gate of the first conductivity typed formed in the substrate adjacent the surface of the substrate, wherein the first region is used as a mask to form a first edge of the first top gate, further wherein the distance between the drain contact region and the first top gate is defined by the lateral length of the first region.

108. The solid state relay circuit of claim 107, wherein each of the drain contact regions of the first and second MOSFETs is formed to extend deeper from the surface of the substrate than the associated top gate, further wherein each drain region is formed with a higher doping density at every depth than an associated top gate.

109. The solid state relay circuit of claim 107, further comprising:

a turn off and gate protection circuit coupled in parallel with photo diode stack to discharge any gate source capacitance when the photo diode stack is not driving voltage to the first and second high voltage MOSFETs.

110. The solid state relay of claim 107, further comprising:

a first switch terminal coupled to the drain of the first high voltage MOSFET; and

a second switch terminal coupled to the drain of the second high voltage MOSFET.

111. A pn junction diode for an integrated circuit comprising:

a substrate;

a first region of relatively thick material formed on a surface of the substrate;

a second region of relatively thick material formed on the surface of the substrate a predetermined lateral distance from the first region;

a first contact of a second conductivity type with high dopant density formed in the substrate adjacent the surface of the substrate, the first contact is positioned between the first and second regions, wherein first edges of the first and second regions are used as a mask to define the edges of the first contact;

a first top gate of a first conductivity type formed in the substrate adjacent the surface of the substrate, a first edge first top gate is adjacent a second edge of the first region, wherein the lateral length of the first region defines the lateral distance between the first top gate and the cathode contact;

a second top gate of the first conductivity type formed in the substrate adjacent the surface of the substrate, a first edge of the second top gate is adjacent a second edge of the second region, wherein the lateral length of the second region defines the lateral distance between the second top gate and the first contact; and

at least one second contact of the first conductivity type with high dopant density formed in the substrate adjacent the surface of the substrate and a predetermined distance from the first top gate.

112. The pn junction diode for an integrated circuit of claim 111, further comprising:

a mid region of the second conductivity type formed in the substrate adjacent the first contact and a portion of each of the first and second top gates, the mid region extending laterally from a portion of the first top gate to a portion of the second top gate, wherein the mid region extends under the first and second regions to create a continuous mid region.

113. The pn junction diode for an integrated circuit of claim 112, wherein the first contact is a cathode contact of a N type conductivity, the second contact is an anode contact of a P type conductivity and the mid region is a cathode region of a N type conductivity.

114. The pn junction diode for an integrated circuit of claim 111, wherein the first and second regions comprise gate material.

115. The pn junction diode for an integrated circuit of claim 111, wherein the first and second regions comprise dielectric material.

116. The pn junction diode for an integrated circuit of claim 115, wherein the first and second regions are formed by local oxidation.

117. The pn junction diode for an integrated circuit of claim 111, wherein end portions of the first and the second relatively thick materials are connected together, the first and the second relatively thick materials having a central opening, the first contact is laterally positioned in the central opening.

118. The pn junction diode for an integrated circuit of claim 117, wherein the first and second top gates extend around an outer perimeter of the first and second relatively thick materials to form a single top gate.

119. A high voltage bipolar transistor for an integrated circuit comprising:

a substrate;

a first region of relatively thick material formed on a surface of a substrate;

a second region of relatively thick material formed on the surface of the substrate a predefined distance from the first region;

a base region of a second conductivity type formed in the substrate, wherein the base region is positioned between the first and second regions; and

a first top gate of a first conductivity type formed in the substrate, wherein the distance between the first top gate and the base region is defined by the lateral length of the first region; and

a second top gate of the first conductivity type formed in the substrate, wherein the distance between the second top gate and the base region is defined by the lateral length of the second region.

120. The high voltage bipolar transistor for an integrated circuit of claim 119, further comprising:

a base contact of the second conductivity type with high dopant density formed in the base region;

an emitter of the first conductivity type with a high dopant density formed in the base region; and

a collector contact of the first conductivity type with high dopant density formed in the substrate a predetermined spaced distance form the base region.

121. The high voltage bipolar transistor for an integrated circuit of claim 119, wherein bipolar transistor is a NPN transistor.

122. The high voltage bipolar transistor for an integrated circuit of claim 119, wherein bipolar transistor is a PNP transistor.

123. The high voltage bipolar transistor for an integrated circuit of claim 119, further comprising:

a drift region of the second conductivity type formed in the substrate, the drift region extending from a portion of the first top gate to a portion of the second top gate.

124. The high voltage bipolar transistor for an integrated circuit of claim 123, wherein the first and second regions are made of a gate material.

125. The high voltage bipolar transistor for an integrated circuit of claim 119, wherein the first and second regions are made of a dielectric material.

126. The high voltage bipolar transistor for an integrated circuit of claim 125, wherein the first and second regions are formed by local oxidation.